



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---------------------------------------------|-------------|----------------------|---------------------|--------------------|
| 10/612,290 | 06/30/2003 | James D. Patterson | 884.910US1 | 5804 |
| 21186 | 7590 | 09/01/2006 | EXAMINER | |
| SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. | | | | SINGH, RAMNANDAN P |
| P.O. BOX 2938 | | | | |
| MINNEAPOLIS, MN 55402 | | | | |
| ART UNIT | | PAPER NUMBER | | |
| | | 2614 | | |

DATE MAILED: 09/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|-----------------------------|---------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/612,290 | PATTERSON, JAMES D. |
| | Examiner Ramnandan Singh | Art Unit 2614 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 June 2006.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-31 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)

6) Other: Final rejection.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed Jun. 22, 2006 have been fully considered but they are not persuasive.

(i) Applicant's argument--“ Fiedler says that a (**common**) differential-to-CMOS level converter 10 is a balanced comparator with differential inputs 12a and 12b [col. 2, lines 63-66]. Thus, Fiedler only refers to one differential circuit” on page 9.

Examiner's response--Examiner respectfully disagrees. It may be noted that Fig. 1 is a schematic diagram of a **common** differential-to-CMOS converter [col. 2, lines 63-64]. Examiner asserts that two complementary outputs, 14a and 14b, cannot be generated using a single differential circuit [Fiedler; col. 2, 63 to col. 3, line 42; Fig. 4, section 70; col. 5, lines 7-40].

(ii) Applicant's argument--“Applicant cannot find any disclosure of, a feedback circuit to monitor the first and second output voltages and apply a bias voltage to lest one of the first and second output drivers” on page 10.

Examiner's response--In response to the above, Applicant is respectfully directed to Fig. 2, wherein cross-over voltage adjustment circuit (36) is a feedback circuit having inputs N8 and complement of N8 derived from the outputs of 34b and 34d respectively [Fig. 2; col. 4, lines 5-39; Fig. 4; col. 5, lines 7-54].

(iii) Applicant's argument---"Applicant can find no disclosure in the cited portion of Fielder to positive and negative conductors of a transmission cable, as cited in claim 3" on page 10.

Examiner's response---Applicant is respectfully directed to Fiedler at col. 8, lines 12-25].

(iv) Applicant's argument---"Applicant cannot find if Fielder any teaching or suggestion of, among other things, a method comprising, providing a correcting bias voltage proportional to a difference between the cross-over voltage and the equidistant voltage, and applying the correcting bias voltage to the differential drivers to vary the voltage point where the first and second output voltages cross-over" on page 10.

Examiner's response--- Applicant is respectfully directed to the rejection of claim 14 as set forth in the Office action dated March 22, 2006, on page 3.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Fiedler [US 5,726,588].

Regarding claim 1, Fiedler teaches an apparatus shown in Fig. 2, comprising:

- a first differential output driver (transistor M1) [Fig. 1] to provide a single ended output voltage (42a) in response to an input voltage (38a);
- a second differential output driver (transistor M2) [Fig. 1] to provide a single ended output (42b) in response to an input voltage (38b), the first output voltage (OUT) and the second output voltage representative of the positive and inverted input voltage [Fig. 2]; and
- a feedback circuit (36) to monitor the first and second output voltages and apply a bias voltage to at least one of the first and second output drivers to vary the point where the first and second output voltages cross-over as the input voltage changes from a first to a second level [col. 4, lines 11-39].

Regarding claim 14, Fiedler teaches a method comprising:

- measuring a difference between a voltage at which output voltage signals of first and second drivers of a differential signal transceiver cross-over and a voltage point substantially equidistant (i.e. **midpoint**) between maximum and minimum output voltages [Figs. 3a-3d; col. 4, line 11 to col. 5, line 5];
- providing a correcting bias voltage proportional to a difference (i.e. offset) between the cross-over voltage and the equidistant voltage (i.e. **midpoint voltage**) [col. 4, lines 11-19]; and
- applying the correcting bias voltage to the differential drivers to vary the voltage point where the first and second output voltages cross-over [col. 4, lines 20-29].

Regarding claim 2, Fiedler further teaches the apparatus, wherein the correcting bias voltage forces the first and second output voltages to cross-over at a point substantially equidistant between maximum and minimum output voltages of the first and second differential drivers [Figs. 3a-3d; col. 4, lines 10-29; col. 4, line 59 to col. 5, line 6].

Regarding claim 3, Fiedler further teaches the apparatus, wherein the first and second output drivers are connected to provide positive and negative outputs to positive and negative conductors of a transmission cable [Fig. 2; col. 3, line 43 to col. 4, line 4; col. 8, lines 12-25].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-12, 15-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiedler as applied to claim 5 above.

Regarding claim 4, Fiedler further teaches the apparatus, wherein the feedback circuit (36) further includes at least one capacitor (72) .

Although Fiedler teaches using feedback circuit (36) for converting the charge of a capacitor into the correcting voltage [Fig. 4; col. 7-27; Figs. 3a-3d; col. 4, lines 40-65], he does not teach expressly a specific method to place a charge, such as using a linear or non-linear method.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place a charge in a linear way such as a charge proportional to a difference between an actual cross-over voltage of the first and second output drivers and the equidistant cross-over voltage (i.e. midpoint voltage) onto the capacitor in order to linearly adjust the cross-over voltage subject to circuit, system and design constraints.

Claim 15 is essentially similar to claim 4 and is rejected for the reasons stated above.

Regarding claim 5, Fiedler further teaches the apparatus,, wherein the at least one capacitor includes a first (72) and second (78) capacitor, wherein the feedback circuit (36) places a charge proportional to a difference between the actual cross-over voltage and the equidistant cross-over voltage onto the first and second capacitors, and wherein the first capacitor supplies a correcting voltage to at least one pull-up bias

circuit in the output drivers, and the second capacitor supplies a correcting voltage to at least one pull down bias circuit in the output drivers [Fig. 4; col. 5, lines 7-54].

Although Fiedler teaches using feedback circuit (36) for converting the charge of a capacitor into the correcting voltage [Fig. 4; col. 7-27; Figs. 3a-3d; col. 4, lines 40-65], he does not teach expressly a specific method to place a charge, such as using a linear or non-linear method.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place a charge in a linear way such as a charge proportional to a difference between an actual cross-over voltage of the first and second output drivers and the equidistant cross-over voltage (i.e. midpoint voltage) onto the capacitor in order to linearly adjust the cross-over voltage subject to circuit, system and design constraints.

Regarding claim 6, Fiedler further teaches the apparatus,, wherein the feedback circuit (36) applies the correcting voltage to increase a drive strength of the pull-up bias circuit (70) and/or to decrease a drive strength of the pull-down bias circuit (84) if the actual cross-over voltage is lower than the equidistant cross-over voltage [Fig. 4; col. 5, lines 7-40].

Regarding claim 7, Fiedler further teaches the apparatus, wherein the feedback

circuit (36) applies the correcting voltage to decrease a drive strength of the pull-up bias circuit (70) and/or to increase the pull-down bias circuit (84) if the cross-over voltage is higher than the equidistant cross-over voltage [Fig. 4; col. 5, lines 7-40].

Claims 16, 17 and 21 are essentially similar to claims 5-7 and are rejected for the reasons stated above.

Regarding claim 8, Fiedler further teaches the apparatus,, wherein the first capacitor (78) provides a correcting voltage to a gate of a PMOS (i.e. P-channel) transistor in the pull-up bias circuit, and wherein the second capacitor (72) provides a correcting voltage to a gate of an NMOS (N-channel) transistor in the pull-down bias circuit [col. 2, lines 3-19; col. 5, line 41-54; col. 7, lines 33-37].

Claim 18 is essentially similar to claim 8 and is rejected for the reasons stated above.

Regarding claim 9, Fiedler further teaches the apparatus,, further including: a differential receiver (32) for detecting a cross-over voltage transition on the differential interface, the differential receiver having a first output [Fig. 2]; a single-ended receiver for detecting rail-to-rail transitions on the positive conductor, the receiver for the positive conductor having a second output [Fig. 2; col. 1, line s17-35]; a single-ended receiver

for detecting rail-to-rail transitions on the negative conductor, the receiver for the negative conductor having a third output [Fig. 2].

Since Fiedler teaches adjusting charges on capacitor (72) and (78) to bring the cross-over voltage [Fig. 4; col. 5, line 41 to col. 6, line 17; col. 7, line 51 to col. 8, line 10], it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply some procedures such as, if the cross-over voltage is lower than the equidistant voltage, charge on the first capacitor is reduced while the first output is high and the second output is low and/or charge on the second capacitor is reduced while the first output is low and the third output is low, in order to optimally adjust the cross-over voltage subject to circuit, system and design constraints.

Regarding claims 10-11, the limitations are shown above.

Claim 20 is essentially similar to claim 11 and is rejected for the reasons stated above.

Regarding claim 12, Fiedler teaches the apparatus, wherein the switches include transmission-gate switches [Fig. 4; col. 5, line 7 to col. 6, line 55].

Regarding claim 22, Fiedler further teaches the apparatus, wherein measuring includes: measuring a cross-over transition on positive and negative conductors of a

transmission cable with the differential signal transceiver; measuring a rail-to-rail transition on the positive conductor of the transmission cable ; measuring a rail-to-rail transition on the negative conductor of the transmission cable; and wherein producing a net charge includes switching a charge onto the capacitor when there is a mismatch in transition times [Figs. 2, 3a-3d; col. 4, lines 5 to col. 5, line 6]

Regarding claims 23-24, the limitations are shown above.

Regarding claim 19, Fielder further teaches the method, wherein the net charge produced is zero) when the cross-over voltage matches the equidistant voltage (i.e. midpoint voltage) [col. 5, lines 41-54].

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Haq and Fiedler as applied to claim 1 above, and further in view of Varma et al [US 6,946,904 B1].

Regarding claim 13, the combination of Haq and Fiedler does not teach expressly a transceiver having a USB interface.

Varma et al a transceiver, wherein the transceiver circuit is an interface to a universal serial bus (USB) [Figs. 1, 4; col. 2, lines 3-18; col. 2, line 59 to col. 3, line 46; col. 7, lines 44-52]

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Varma et al with Komarek et al and Haq in order to protect transceivers from over-voltages [Varma et al; col. 2, lines 17-18].

7. Claims 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haq [US 6,430,606 B1] in view of Fiedler [US 5,726,588].

Regarding claim 25, Haq teaches a system shown in Figs 22A and 22B, comprising:

a transceiver (2200) interface coupled to a differential communication bus, the transceiver interface having a differential cross-over voltage of a magnitude between high and low transceiver output voltages [Figs. 21, 22A-22C, 23A-23B; col. 20, line 27 to col. 21, line 15]; and

a transceiver controller (2502) in communication with the transceiver interface [Figs. 24-26; col. 21, line 18 to col. 24, line 8].

Although Haq teaches a crossover voltage [col. 10, line 50 to col. 11, line 5; col. 12, lines 30-53], he does not teach expressly a cross-over lock feedback circuit to correct deviations of the cross-over voltage.

Fiedler teaches a cross-over lock feedback circuit (36) to correct deviations of the cross-over voltage from a voltage point equidistant between maximum and minimum output voltages of the transceiver (32) [Figs. 1-2, 31-3d; col. 4, line 5 to col. 5, line 6].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Fiedler with Haq in order to provide a cross-over voltage adjustment to an optimum level [Fiedler; col. 4, lines 24-39].

Claim 29 is essentially similar to claim 25 except for a processor in communication with the transceiver controller; and a DRAM memory in communication with the processor. Haq further teaches a processor (i.e. a master or memory controller 1305) in communication with the transceiver controller 2502 [Figs. 13A, 22C] ; and a DRAM memory in communication with the processor [col. 6, lines 11-26; col. 13, lines 24-44; col. 13, line 66 to col. 14, line 60].

Regarding claim 26, Fiedler further teaches the system, wherein the transceiver interface includes at least one transceiver driver coupled to the cross-over lock feedback circuit [Fig. 2], the driver having a pull-up circuit (70) and a pull-down circuit (84) [Fig. 4; col. 5, lines 7-40; col. 2, lines 3-30]; and wherein the feedback circuit (36) feeds back a correcting voltage to the driver to adjust the pull-up and/or pull-down of the driver to correct the cross-over voltage [Fig. 4; col. 4, lines 11-58].

Claim 30 is essentially similar to claim 26 and is rejected for the reasons stated above.

Regarding claim 27, Fiedler further teaches the system, wherein the cross-over lock feedback circuit (36) produces a charge in proportion to a difference of the cross-over voltage from the equidistant voltage (i.e. **midpoint voltage**) to provide the correcting voltage [col. 4, lines 11-19].

Claim 31 is essentially similar to claim 27 and is rejected for the reasons stated above.

Regarding claim 28, Haq further teaches the apparatus , including: a differential receiver (210) for detecting a cross-over voltage transition on the differential interface, the differential receiver having a first output [Fig. 6B]; a single-ended receiver (405) for detecting rail-to-rail transitions on the positive conductor, the receiver for the positive conductor having a second output; a single-ended receiver (405) for detecting rail-to-rail transitions on the negative conductor [Fig. 4], the receiver for the negative conductor having a third output [Fig. 4; col. 7, line 49 to col. 8, line 60].]

Although Haq teaches a crossover voltage [col. 10, line 50 to col. 11, line 5; col. 12, lines 30-53], he does not teach expressly a cross-over lock feedback circuit to correct deviations of the cross-over voltage.

Fiedler teaches the feedback circuit (36) produces a charge based on asymmetry of switching times at receiver outputs when the cross-over voltage is different from the midpoint voltage [Figs. 3a-3d; col. 4, line 5 to col. 5, line 6].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Fiedler with Haq in order to provide a cross-over voltage adjustment to an optimum level [Fiedler; col. 4, lines 24-39].

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramnandan Singh whose telephone number is (571) 272-7529. The examiner can normally be reached on M-TH (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fan Tsang can be reached on (571) 272-7547. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ramnandan Singh
Examiner
Art Unit 2614



FAN TSANG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600